IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A voltage supply circuit, comprising:

a first transistor ~~(21)~~ having a first main electrode coupled to a power supply, a second main electrode, and a control electrode that is not directly connected to ground; and

a second transistor ~~(22)~~ having a ~~first~~ third main electrode coupled to the second main electrode of the first transistor ~~(21),~~ and a ~~second~~ fourth main electrode for supplying a regulated voltage, the ~~second~~ fourth main electrode being coupled to the control electrode ~~(26)~~ of the first transistor ~~(21)~~.

2. (Currently Amended) A circuit according to claim 1, wherein the first transistor ~~(21)~~ is a junction field effect transistor ~~JFET~~.

3. (Currently Amended) A circuit according to claim 2, wherein the second transistor ~~(22)~~ is a junction field effect transistor ~~JFET~~.

4. (Currently Amended) A circuit according to claim 1, wherein a gate ~~(25)~~ of the second transistor ~~(22)~~ is connected to ground.

5. (Currently Amended) A circuit according to claim 1, wherein the first transistor ~~(21)~~ is formed by a silicon-on-insulator (SOI) integration technology.

6. (Currently Amended) A circuit according to claim 1, wherein the second transistor ~~(22)~~ is formed by a silicon-on-insulator (SOI) integration technology.

7. (Currently Amended) A circuit according to claim 1, wherein the first transistor ~~(21)~~ is a high voltage junction field effect transistor ~~JFET~~ and the second transistor ~~(22)~~ is a low voltage junction field effect transistor ~~JFET~~.

8. (Currently Amended) A circuit according to claim 1, further comprising a load ~~(24, 30)~~ coupled to the second main electrode of the second transistor ~~(22)~~ to receive the regulated voltage.

9. (New) A circuit according to claim 8, wherein the load comprises a capacitor and a current source.

10. (New) A voltage supply circuit, comprising:

a first transistor having a first electrode coupled to a power supply, a first gate, and a second electrode; and

a second transistor having a third electrode coupled to the second electrode, a second gate, and a fourth electrode coupled to the first gate of the first transistor, the fourth electrode operable to supply a regulated voltage.

11. (New) The voltage supply circuit of Claim 10, further comprising a load coupled to the fourth electrode of the second transistor, the load operable to receive the regulated voltage.

12. (New) The voltage supply circuit of Claim 11, wherein multiplication current from the first gate of the first transistor is fed into a current path of the fourth electrode of the second transistor.

13. (New) The voltage supply circuit of Claim 10, wherein the second gate is coupled to ground.

14. (New) The voltage supply circuit of Claim 10, wherein the first and second transistors comprise junction field effect transistors.

15. (New) The voltage supply circuit of Claim 10, wherein the first and second transistors are formed by a silicon-on-insulator (SOI) integration technology.

16. (New) A method, comprising:

coupling a first electrode of a first transistor to a power supply;

coupling a second electrode of the first transistor to a third electrode of a second transistor;

coupling a fourth electrode of the second transistor to a first gate of the first transistor; and

coupling the fourth electrode of the second transistor to a load, the fourth electrode operable to supply a regulated voltage to the load, wherein multiplication current from the first gate of the first transistor is fed into a current path of the fourth electrode of the second transistor.

17. (New) The method of Claim 16, further comprising coupling a second gate of the second electrode to ground.

18. (New) The method of Claim 16, wherein the load comprises a capacitor and a current source.

19. (New) The method of Claim 16, wherein the first and second transistors comprise junction field effect transistors.

20. (New) The method of Claim 16, wherein the first and second transistors are formed by a silicon-on-insulator (SOI) integration technology.